Multilevel Single-Phase Converter with Two DC Links

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Abstract—In this paper, a multilevel single-phase converter is proposed and investigated. Its structure is based on cascaded-transformer systems, which are very interesting in applications in which a single dc source is available. The features of well-known multilevel cascaded H-bridge and transformer-based solutions are integrated into the proposed converter. As a result, the number of synthesized voltage levels can be optimized without excessively increasing the number of transformers. The basic configuration has six two-level IGBT legs, two injection transformers, and two dc links (the lowest voltage dc link may be a floating capacitor or be connected to a small dc power source). The configuration is generalized and the calculation of the transformers turns ratios as well as the dc-link voltages to maximize the number of voltage levels is provided. The proposed configuration is compared with cascaded H-bridge and a single-phase shared leg converter, which are also cascaded by means of transformers. Compared with the conventional converters, the proposed one has lower switching losses and higher conduction losses. Thus, the proposed configuration is more interesting in terms of semiconductor losses for high-voltage and low-current applications. Experimental and simulation results are shown to demonstrate the feasibility of the system.

Index Terms—cascaded systems, harmonic distortion, inverters, multilevel systems, transformers.

I. INTRODUCTION

Multilevel Voltage Source Converters (VSCs) are one of the preferred choices of electronic power conversion for high-power medium-voltage applications. These converters have high-quality output voltages, which can reduce the filter size (or even avoid the utilization of filters) [1]. They also have great power and voltage capabilities [2], being an enabling technology for high-voltage applications.

One of the most known VSC topology is the cascaded H-bridge (CHB) [3]. This configuration has received great attention in very high-power and power-quality applications,

primarily due to its modularity [4]. In CHB systems, each H-bridge unit requires an isolated and independent dc source, while the number of output voltage levels can be manipulated by specific dc-link ratio [5].

Inverters cascaded by means of line frequency transformers (LFTs) [6], [7] and topologies with high-frequency transformers (HFTs) [8], [9] have been proposed and investigated in the literature. Inverters with LFTs and a single dc source demand simpler control of the dc-link voltage, when required [10], than configurations with several dc links. Besides, the appropriate selection of the transformers turns ratios improves the number of generated voltage levels [11]. This type of configuration has been applied, for example, as a series compensator [12], active power filter [13], [14], and inverter [15]–[22].

In order to avoid the utilization of several dc sources, the H-bridges of CHB can be cascaded using injection transformers. In this case, a single dc source is needed and the transformers turns ratios can be utilized to improve the number of output voltage levels. This converter is represented in Fig. 1a and was proposed in [23]. Configurations with a reduced number of components (when compared to CHB), a single dc link, and injection transformers are proposed and discussed in [17]–[19].

A generalized single-phase shared leg converter is proposed in [16]. This converter is shown in Fig. 1b and is named here as Cascaded Shared Leg One DC Link (CSL-1D). CSL-1D provides more levels per leg than CHB, but has more transformers.

This paper proposes a generalized single-phase topology with two dc links and two shared legs. This topology is shown in Fig. 1c and is named here as Cascaded Shared Legs Two DC Links (CSL-2D). Conventional and proposed topologies operate with LFTs. [24] proposes an inverter with injection transformers and two dc links (one is a floating capacitor) that has more transformers than CSL-2D. All the analyses presented in this paper consider the asymmetrical operation of the topologies. This means that the transformers turns ratios and the dc-link voltages ratio (in the case of CSL-2D) are chosen to maximize the number of voltage levels of the generated voltages. The transformer that transfers most of the power for each topology is highlighted in Fig. 1 and might be removed when isolation is not required (the connections when the transformer is removed are also represented in the figures). For example, CSL-2D with six legs can operate with a transformer handling only 30% of the load power.

The studied configurations are analyzed in this paper as inverters. However, they could also be applied as rectifiers,
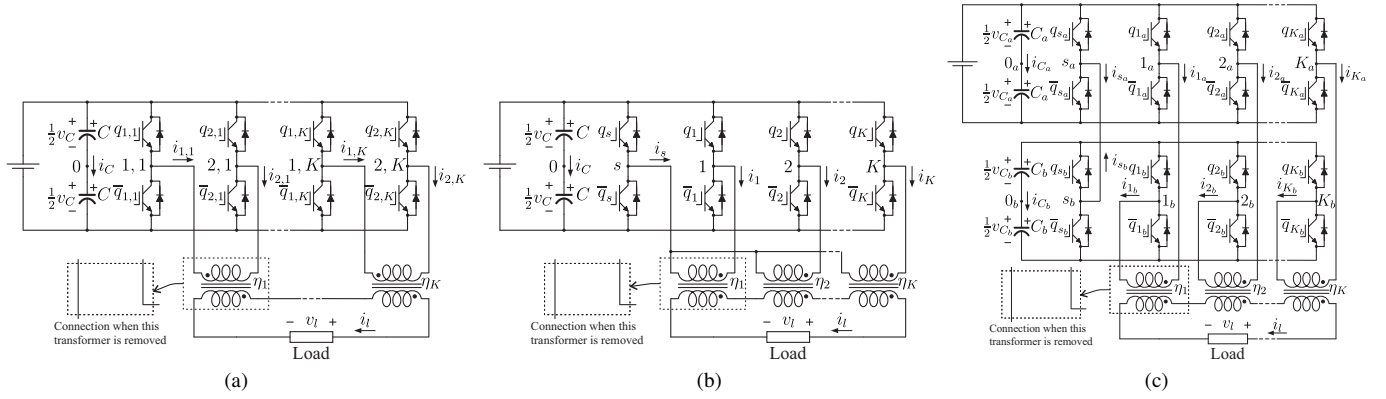
Fig. 1. Conventional (a and b) and proposed (c) topologies. (a) Cascaded H-bridge (CHB) with injection transformers and one dc link. (b) Cascaded Shared Leg One DC Link (CSL-1D). (c) Cascaded Shared Legs Two DC Links (CSL-2D).

Dynamic Voltage Restorers (DVRs), and series filters. A comparative analysis of the investigated configurations with six legs is performed by means of simulations. The rating of the components, harmonic distortions of the generated voltages, semiconductor losses and switching frequencies are analyzed. The number of components is also compared. A generalized model of CSL-2D is presented followed by the calculation of its parameters in order to maximize the number of equally spaced voltage levels. Simulation and experimental results in many situations are provided to demonstrate the feasibility of the proposed system.

As the advantages of the proposed topology, the following points can be highlighted 1) Compared with CHB and CSL-1D, CSL-2D has more levels per transformer/leg when the configurations have the same number of legs/transformers; 2) CSL-2D has lower switching and higher conduction losses than the conventional topologies, being more interesting for applications with high voltages and low currents; 3) CSL-2D has fewer transformers than the conventional topologies (this might reduce the system cost). Another point to emphasize is that, although CSL-2D has two dc links, the one with the lowest voltage can be a floating capacitor and a technique to regulate this capacitor voltage is included in the paper.

II. SYSTEM MODEL

CSL-2D is based on CHB cells along with cascaded-transformer inverters. The proposed converter uses two dc links, two shared legs, and legs cascaded by means of injection transformers, as shown in Fig. 1c. The CSL-2D inverter increases the degrees of freedom of a multilevel system, since the transformers turns ratio and dc-links ratio can be manipulated to optimize the number of synthesized voltage levels. Furthermore, CSL-2D might operate with a single dc source. On the other hand, the existing multilevel solutions require either several isolated dc sources or several injection transformers. The description of the proposed system is given in this section.

N_{leg} and N_{trf} are defined as the number of legs and injection transformers of a given topology, respectively. Thus, CSL-2D has $N_{leg}/2-1$ transformers and utilizes two dc links to supply a load with voltage and current given by v_l and i_l, respectively. Moreover, each dc link comprises $N_{leg}/2$ legs.

Consider that q_{w_n} represents the state of the upper switch of the leg w_n (the states of upper and bottom switches are complementary), where $w = s$ or $w = k = 1, 2, ..., N_{leg}/2-1$ and $n = a, b$. Legs s_a and s_b are connected, while legs k_a and k_b are connected to the primary terminals of an injection transformer whose turns ratio is η_k. When $q_{w_n} = 1$, the switch is on, while when $q_{w_n} = 0$, the switch is off.

The pole voltages can be calculated by $v_{w_n 0_n} = (2q_{w_n} - 1)\frac{v_{C_n}}{2}$, where the converter pole voltage $v_{w_n 0_n}$ is the voltage between the point w_n and the dc-link midpoint (point 0_n) and v_{C_n} is the voltage of the dc link n.

The generated voltage is written as a function of the pole voltages and the transformers turns ratios as follows:

$$v_l = v_{l_a} - v_{l_b} \tag{1}$$

where $v_{l_a} = \sum_{k=1}^{K} \eta_k v_{k_a 0_a} - \eta_s v_{s_a 0_a}$, $v_{l_b} = \sum_{k=1}^{K} \eta_k v_{k_b 0_b} - \eta_s v_{s_b 0_b}$, $K = N_{leg}/2 - 1$, η_k is the turns ratio of the injection transformer whose primary terminals are connected to points k_a and k_b, and $\eta_s = \sum_{k=1}^{K} \eta_k$.

According to (1), the load voltage depends on η_k and v_{C_a}/v_{C_b}, which are defined to obey design rules. A detailed discussion about how these parameters can be calculated is given in the next section.

i_{w_n} represents the current flowing out of leg w_n. The leg currents can obtained according to η_k and the load current, which are given by $i_{s_a} = -\eta_s i_l$, $i_{s_b} = \eta_s i_l$, $i_{k_a} = \eta_k i_l$, and $i_{k_b} = -\eta_k i_l$. It can be noted that another feature of η_k is to define the switch current ratings.

III. PARAMETERS CALCULATION

The transformers turns ratios and the dc-link voltages are related with many characteristics of the inverter. In this paper, these parameters are calculated in order to maximize the number of equally spaced voltage levels. The basic unit of the proposed topology has $N_{leg} = 6$, as the converter with $N_{leg} = 4$ is equivalent to the CHB with two H-bridges connected in series. However, the generalization here presented is valid for the topology with any even $N_{leg} \geq 4$.

The turns ratio η_k is here defined in terms of two components, η_p and η_{k_s} (η_p is the number of turns in the primary

TABLE I
CONVERTER PARAMETERS

Parameter	CSL-2D	CSL-1D	CHB
N_{leg}	$4 + 2n$	$2 + n$	$2n$
N_{trf}	$N_{leg}/2 - 1$	$N_{leg} - 1$	$N_{leg}/2$
N_{lvl}	$\left(2^{N_{leg}/2} - 1\right)^2$	$2^{N_{leg}} - 1$	$3^{N_{leg}/2}$
η_k	$\dfrac{2^{\left(N_{leg}/2-1-k\right)}}{2^{\left(N_{leg}/2-1\right)}-1}$	$\dfrac{2^{\left(N_{leg}-1-k\right)}}{2^{\left(N_{leg}-1\right)}-1}$	$\dfrac{2 \cdot 3^{\left(N_{leg}/2-k\right)}}{3^{N_{leg}/2}-1}$
v_{C_a}/v_{C_b}	$2^{N_{leg}/2} - 1$	-	-

n is any integer such $n \geq 1$.

side of all transformers, while η_{k_s} is the number of turns in the secondary side of the transformer T_k), such $\eta_k = \eta_{k_s}/\eta_p$. The maximum amplitude of v_l produced by the converter is $V_{l_{max}}$, and the rms value of the load voltage is V_l. The modulation index of the converter m_a is defined as the ratio between the amplitude of the load voltage $\sqrt{2}V_l$ and the maximum voltage generated by the converter $V_{l_{max}}$. Thus, $0 < m_a \leq 1$.

N_{lvl} is the maximum number of equally spaced voltage levels (considering $m_a = 1$) that can be generated across the load by a given configuration with specific parameters. Considering CSL-2D, N_{lvl} is maximized when

$$\eta_{k_s} = 2^{(K-k)} \qquad v_{C_a} = (2^{N_{leg}/2} - 1)v_{C_b} \qquad (2)$$

and, in this case,

$$N_{lvl} = \left(2^{N_{leg}/2} - 1\right)^2. \qquad (3)$$

$V_{l_{max}}$ is calculated as $V_{l_{max}} = \eta_s(v_{C_a} + v_{C_b})$. If η_p is calculated as $\eta_p = \sum_{k=1}^{K} \eta_{k_s}/g$, η_s will be equal to g (as $\eta_s = \sum_{k=1}^{K} \eta_k$). Consequently, $V_{l_{max}} = g(v_{C_a} + v_{C_b})$. In all comparisons presented in this paper, $g = 1$. However, this parameter can assume other values and increase or decrease $V_{l_{max}}$. If isolation is not required, one transformer can be removed. In this case, if the transformer T_1 is removed, the turns ratios of the other transformers will be calculated as the original values divided by η_1 and the dc-link voltages will be calculated as the original values multiplied by η_1.

As an example, consider the topology with $N_{leg} = 6$ and $g = 1$. $\eta_{1_s} = 2$ and $\eta_{2_s} = 1$ are obtained from (2). Then $\eta_p = (\eta_{1_s} + \eta_{2_s})/g = 3$ and thus $\eta_1 = 2/3$ and $\eta_2 = 1/3$ (transformers turns ratios). Using (2), the dc-link voltage ratio is calculated as $v_{C_a} = 7v_{C_b}$. Then $N_{lvl} = 49$ is obtained from (3). The number of voltage levels can be reduced using different dc-link voltage ratios to increase the number of voltage level redundancies (e.g., when $v_{C_a} = 6v_{C_b}$, $N_{lvl} = 43$ and, when $v_{C_a} = 5v_{C_b}$, $N_{lvl} = 37$). These redundancies can be selected to reduce the switching frequency of the converter.

η_k and v_{C_a}/v_{C_b} can also be selected to improve the converter symmetry. In this case, when $N_{leg} = 6$, all the transformers have the same turns ratio ($\eta_1 = 1/2$ and $\eta_2 = 1/2$), the dc-link voltages are equal ($v_{C_a} = v_{C_b}$), and the topology generates up to 9 levels. The symmetric operation becomes more interesting when it is desired to minimize the rating of the components.

IV. GENERAL CONFIGURATIONS COMPARISON

In this section, the configurations are compared in terms of several characteristics. Table I shows the main parameters of the converters as well as the corresponding parameters to maximize N_{lvl}. CSL-2D has twice the number of dc links of the conventional configurations. However, its dc link with the lowest voltage can be a floating capacitor (i.e., not be connected to a voltage supply). Besides, this configuration has the lowest number of transformers for the same number of legs. The lower expenses with transformers may overcome the cost of the second dc link.

[16] presents a methodology to calculate the parameters of CHB and CSL-1D such as N_{lvl} is maximized. $V_{l_{max}} = v_C$ for the conventional configurations and $V_{l_{max}} = v_{C_a} + v_{C_b}$ for the proposed one. The transformers voltage ratings for all topologies are $V_{l_{max}}$.

Table I compares the configurations in terms of N_{lvl}, transformers turns ratios and dc-link voltage ratio (in the case of CSL-2D). For CHB, K is the number of H-bridges, k represents the H-bridge such $k = \{1, 2, ..., K\}$, $1, k$ and $2, k$ represent the two legs of the H-bridge k, and η_k is the turns ratio of the transformer connected to the H-bridge k. For CSL-1D, K is the number of non-shared legs, s represents the shared leg, while k represents the non-shared legs such $k = \{1, 2, ..., K\}$, and η_k is the turns ratio of the transformer whose primary terminals are connected to legs s and k.

The topologies can also be compared considering the ratings. Table II provides the voltage (V_{rat}) and current (I_{rat}) ratings of the switches, respectively, in the condition analyzed.

TABLE II
SWITCH CURRENT (I_{rat}) AND VOLTAGE (V_{rat}) RATINGS, AS A FRACTION OF i_l AND $V_{l_{max}}$

	CSL-2D		CSL-1D		CHB
	s_a/s_b	k_a/k_b	s	k	$1, k/2, k$
I_{rat}	1	$\dfrac{2^{\left(N_{leg}/2-1-k\right)}}{2^{\left(N_{leg}/2-1\right)}-1}$	1	$\dfrac{2^{\left(N_{leg}-1-k\right)}}{2^{\left(N_{leg}-1\right)}-1}$	$\dfrac{2 \cdot 3^{\left(N_{leg}/2-k\right)}}{3^{N_{leg}/2}-1}$
	w_a	w_b	any		any
V_{rat}	$\dfrac{2^{N_{leg}/2}-1}{2^{N_{leg}/2}}$	$\dfrac{1}{2^{N_{leg}/2}}$	1		1

The converters whose legs are connected to v_{C_a} and v_{C_b} are named converters a and b, respectively. As shown in Table II, one of CSL-1D legs will process all the load current. In the case of CHB, this does not happen. Its switches always process a fraction of the load current. Considering CSL-2D, two of its legs process all the load current. Besides, the legs of converters a and b are in series ($i_{sa} = -i_{sb}$ and $i_{ka} = -i_{kb}$). CHB and CSL-1D do not have series connected legs. Consequently, CSL-2D will have higher conduction losses.

As shown in Table II, CSL-2D has the lowest switch voltage rating. The switches of converter b have a significantly lower voltage rating than the ones of converter a. The PWM strategy can be implemented to minimize the switching frequency of converter a and reduce the switching losses of the topology.

Fig. 2 shows the maximum number of levels per transformer/leg when the configurations have the same number of legs/transformers. The same figure also shows V_{rat} in each

leg per transformer/leg when the configurations have the same number of legs/transformers. CSL-2D has the best results in terms of number of levels. On the other hand, CSL-1D has a better result than CHB when both topologies have the same number of legs, while the opposite happens when both topologies have the same number of transformers. Considering V_{rat}, CSL-2D has the best results because its switches only process part of the rated voltage of the system.

V. UNIDIMENSIONAL (1-D) MODULATION TECHNIQUE

Fig. 3 shows the representation of the voltage levels, auxiliary variables v_{l_a} and v_{l_b}, and respective switching combinations generated by CSL-2D with $N_{leg} = 6$. In this case, $\eta_1 = 2/3$, $\eta_2 = 1/3$, $v_{C_a} = 7v_{C_b}$, and $N_{lvl} = 49$. $V_x = \frac{x}{24}v_{C_t}$, x is an integer between -24 and 24, $v_{C_t} = v_{C_a} + v_{C_b}$ and Q_{n_a,n_b} represents a switching combination, where n_a and n_b are the binary numbers $q_{1_a}q_{2_a}q_{s_a}$ and $q_{1_b}q_{2_b}q_{s_b}$, respectively, converted to decimal numbers. For example, if $q_{1_a} = 0$, $q_{2_a} = 1$, and $q_{s_a} = 1$, $n_a = 3$.

Only the voltage levels with $v_l \geq 0$ are represented in Fig. 3 given that they are symmetric with respect to 0. This means that V_{-x} is generated by switching combinations complementary to the combinations that generate V_x. For example, as $Q_{6,1}$ generates V_{24}, V_{-24} is generated by $Q_{1,6}$.

v_l^* represents the voltage to be generated by the converter. The reference voltage should be synthesized by the voltage levels V_y and V_z such $V_y \leq v_l^* \leq V_z$. Usually, these voltage levels are the ones closest to v_l^* as this reduces the harmonic distortion of the generated voltage. However, the utilization of non-consecutive voltage levels sometimes is interesting. To implement the technique, it can be written that $v_l^* = \frac{t_y}{T}V_y + \frac{t_z}{T}V_z$ and $T = t_y + t_z$, where t_y and t_z are the application times of the voltage levels V_y and V_z, respectively.

VI. FLOATING CAPACITOR REGULATION

The instantaneous load power p_l and the instantaneous powers in dc links a and b, p_{C_a} and p_{C_b}, are given by
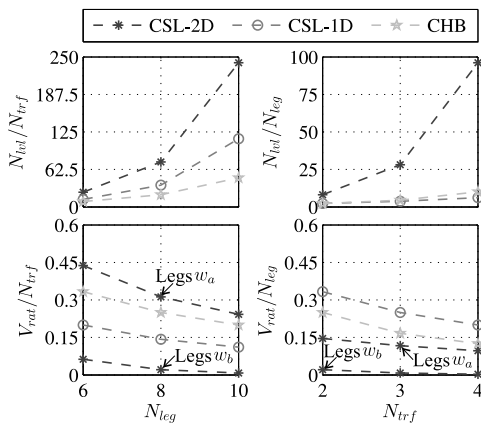
$$p_l = v_l i_l = -p_{C_a} - p_{C_b} \tag{4}$$

where $p_{C_a} = -v_{l_a} i_l$ and $p_{C_b} = v_{l_b} i_l$.

A positive/negative instantaneous power means the dc link is receiving/giving power at the considered instant. In this section, CSL-2D is analyzed with $N_{leg} = 6$ and $N_{lvl} = 49$ (see Fig. 3). As v_{C_b} is small compared with v_{C_a} ($v_{C_a} = 7v_{C_b}$), the operation of dc link b as a floating capacitor is interesting.

As one can see in Fig. 3, the voltage levels are generated by a unique combination of the auxiliary variables v_{l_a} and v_{l_b}. This means that a voltage level does not have redundancies in terms of p_{C_a} and p_{C_b}. In this case, non-consecutive voltage levels may be utilized to regulate v_{C_b}.

The voltage levels that contribute to increase/decrease v_{C_b} are the ones in which p_{C_b} is positive/negative. In the beginning of the sampling period, v_{C_b} is compared with its reference value $v_{C_b}^*$. If this voltage is within the tolerable balancing range (or hysteresis band), v_l is synthesized using the two closest voltage levels. Otherwise, in order to decide which voltage levels to utilize to increase/decrease v_{C_b}, the following steps are done:
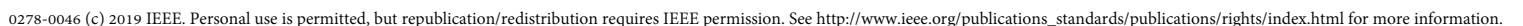
- Step 1: select the two closest voltage levels that can synthesize v_l^*.
- Step 2: does one of these voltage levels generate a positive/negative p_{C_b} and does the other generate a positive/negative or equals zero p_{C_b}? If yes, use these levels to increase/decrease v_{C_b}. If no, go to the next step.
- Step 3: exchange one of these voltage levels by the closest voltage level that can synthesize v_l^* with a lower/higher value of p_{C_a} (if such voltage level cannot be found, v_{C_b} cannot be increased/decreased at this moment and the voltage levels from step 1 should be used). Is a slow increase/decrease of v_{C_b} needed? If yes, use these voltage levels. If no, go to the next step.
- Step 4: select the two closest voltage levels that can synthesize v_l^* with $v_{l_b} = v_{C_b}$ / $v_{l_b} = -v_{C_b}$, when $i_l \geq 0$, or $v_{l_b} = -v_{C_b}$ / $v_{l_b} = v_{C_b}$, when $i_l < 0$. Use these voltage levels to promote a fast increase/decrease of v_{C_b}.

For example, consider that $\frac{19}{24}v_{C_t} \leq v_l^* \leq \frac{20}{24}v_{C_t}$ and i_l is positive. The two closest voltage levels that synthesize v_l^* are V_{19} and V_{20} (step 1). If v_{C_b} should increase, V_{19} and V_{20} can be used (step 2). If v_{C_b} should decrease: V_{19} and V_{20} cannot be used (step 2). V_{19} can be replaced by V_{17} to provide a slow decrease of v_{C_b} (step 3). V_{17} and V_{24} can be utilized to promote a fast decrease of v_{C_b} (step 4).

Using the steps 1 to 4, the floating dc link (v_{C_b}) is regulated by properly choosing switching combinations that control the power flow direction. The PWM strategy performs the mechanism to define the switching combinations, which are established prior to the implementation of the converter. Thus, the regulation algorithm can be done in a short computation time, once there are no complex real-time calculations.

P_{C_a} and P_{C_b} represent the mean power of dc links a and b, respectively, during a complete cycle of v_l. A steady-state analysis of CSL-2D with 1-D modulation using the closest voltage levels over several modulation indexes was done. The results of CSL-2D with $N_{leg} = 6$ and $N_{lvl} = 49$ are shown in Fig. 4. This figure shows P_{C_b} versus m_a, normalized in relation to the load power P_l. The operating points in which $P_{C_b} = 0$ are highlighted. In these points, all the load power

Fig. 2. N_{lvl}/N_{trf} versus N_{leg} (top-left), N_{lvl}/N_{leg} versus N_{trf} (top-right), V_{rat}/N_{trf} versus N_{leg} (bottom-left), and V_{rat}/N_{leg} versus N_{trf} (bottom-right).

is processed by dc link a. This situation is interesting when dc link b is a floating capacitor because v_{C_b} will be naturally regulated (i.e., no regulation strategy will be needed most of the time) and dc link b will contribute only with the generation of the voltage levels.

Fig. 4. Mean power of dc link b versus m_a (CSL-2D with $N_{leg} = 6$ and $N_{lvl} = 49$).

Steady-state analyses of CSL-2D operating with $N_{leg} = 6$ and an intermediate N_{lvl} (43 and 37) were also done. In these cases, some voltage levels have redundancies in terms of v_{l_a} and v_{l_b} (i.e., redundancies in terms of p_{C_a} and p_{C_b}) that can be utilized to regulate the floating capacitor voltage. With $N_{lvl} = 43$ ($v_{C_a} = 6v_{C_b}$) and $N_{lvl} = 37$ ($v_{C_a} = 5v_{C_b}$), v_{C_b} can be regulated using only voltage level redundancies when $0.45 \leq m_a \leq 0.93$ and $m_a \leq 0.99$, respectively. As already explained, there are no voltage level redundancies when $N_{lvl} = 49$.

Simulations were also done to verify if the floating capacitor could be regulated with any modulation index and load power factor using distant voltage levels, when necessary. The floating capacitor of CSL-2D with $N_{lvl} = 49$ and 43 can be regulated for any m_a (CSL-2D with $N_{lvl} = 37$ can regulate the floating capacitor when $m_a \leq 0.99$).

When generating 49 levels and $N_{leg} = 6$, the operation of CSL-2D with two dc power sources is reasonable, as the power processed by dc link b is low (when $m_a \geq 0.75$, the power processed by dc link b is always lower than 4.4% of P_l). In this case, no floating capacitor regulation needs to be done and the closest voltage levels are always utilized.

VII. CONFIGURATIONS COMPARISON WITH $N_{leg} = 6$

In this section, a comparative analysis of the investigated topologies with $N_{leg} = 6$ is performed. The conventional topologies operate with N_{lvl} maximized (i.e., their parameters are calculated according to the equations in Table I) and CSL-2D operates with N_{lvl} equals 49, 43, and 37 ($v_{C_a} = 7v_{C_b}$, $v_{C_a} = 6v_{C_b}$, and $v_{C_a} = 5v_{C_b}$, respectively).

Table III shows the system parameters used in the analysis and the converter parameters are calculated based on Table I. It is worth noting that, for the same system parameters, each studied topology has different switches, dc links, and

transformers ratings. All configurations were implemented using 1-D modulation. The voltage levels are applied symmetrically with respect to half of the sampling interval and the redundancies are selected so the switching frequency is minimized.

TABLE III
SYSTEM PARAMETERS USED IN THE ANALYSIS

Parameter		Value
Reference load voltage	V_l^*	220 V(rms)
Modulation index	m_a	1
Load power	P_l	500 W
Load power factor	$\cos\varphi$	0.99
Load frequency	f_l	60 Hz
Sampling frequency	f_s	10.02 kHz *

* This value is modified in the losses analysis.

A. Components Rating

The voltage rating of the switches are represented in Table IV and are normalized in relation to $V_{l_{max}}$ ($V_{l_{max}} = v_{C_a} + v_{C_b}$ for CSL-2D and $V_{l_{max}} = v_C$ for CHB and CSL-1D). As $m_a = 1$, $V_{l_{max}} = \sqrt{2}V_l^*$. The switches whose legs are connected to dc links a and b have voltage ratings v_{C_a} and v_{C_b}, respectively. For example, the voltage rating of the converter a (legs w_a) when $v_{C_a} = 7v_{C_b}$ is $\frac{v_{C_a}}{v_{C_a} + v_{C_b}} = 87.5\%$ of $V_{l_{max}}$. Considering CSL-1D and CHB, the dc-link voltage is v_C and, consequently, the voltage rating of all switches is v_C (100% of $V_{l_{max}}$). As one can see, CSL-2D has switches with the lowest voltage rating.

The current rating for the switches of each leg was also computed. Table V shows the current rating for the switches of each leg, normalized with respect to the load current. These results agree with the equations given in Table II.

TABLE IV
VOLTAGE RATING FOR THE SWITCHES OF EACH LEG (%), NORMALIZED
IN RELATION TO $V_{l_{max}}$

Leg	CSL-2D ($N_{lvl} = 49/43/37$)	CSL-1D	CHB
w_a/all/all	87.5/85.71/83.33	100	100
w_b	12.5/14.29/16.67	-	-

Considering CSL-2D, as converters a and b are in series, the current rating of legs w_a and w_b is the same. Besides, the shared legs s_a and s_b process 100% of the load current. CSL-1D has the leg s processing 100% of i_l, but the other legs have a parallel connection behavior and each leg processes a

Fig. 3. Representation of the voltage levels generated by CSL-2D with $N_{leg} = 6$ and $N_{lvl} = 49$ ($v_l \geq 0$).

different portion of i_l. CHB legs process only a portion of i_l. Consequently, in terms of switches current rating, CHB and CSL-1D have the best performance. These results do not depend on the load power factor or modulation index.

TABLE V
CURRENT RATING FOR THE SWITCHES OF EACH LEG (%), NORMALIZED IN RELATION TO i_l (CSL-2D WITH $N_{lvl} = 49, 43,$ AND 37)

Topology	Leg					
	$s_a/s/$ $1,1$	$1_a/1/$ $2,1$	$2_a/2/$ $1,2$	$s_b/3/$ $2,2$	$1_b/4/$ $1,3$	$2_b/5/$ $2,3$
CSL-2D	100	66.67	33.33	100	66.67	33.33
CSL-1D	100	51.61	25.81	12.90	6.45	3.23
CHB	69.23	69.23	23.08	23.08	7.69	7.69

The transformers voltage ratings are the same for all the topologies, $v_{C_t} = 312$ V. The mean power transferred by the transformers T_1 and T_2 of CSL-2D is around 70% and 30% of the load power, respectively. In CHB, T_1 processes almost all the load power, which is 82.68%. While in CSL-1D the power processed by $T_1, T_2, T_3, T_4,$ and T_5 is 58.88%, 24.41%, 10.78%, 3.68%, and 2.25% of the load power, respectively. These values do not depend on the power factor, however they depend on m_a and the PWM technique.

A high number of transformers can considerably increase the total volume of the converter. Besides, the power processed is an important parameter for the size of a transformer. C2L-2D is a good option because it has a low number of transformers (unlike CSL-1D) and the power is not mostly concentrated in only one transformer as the case of CHB. Therefore, CSL-2D might have a higher power density than the conventional multilevel structures analyzed in this paper. Proposed and conventional topologies can have one transformer less when isolation is not a system requirement (in this case, the transformer of CSL-2D that transfers almost 70% of the power can be removed).

B. Generated Voltages and Harmonic Distortions

Fig. 5 shows the generated voltages of CHB (27 levels), CSL-1D (63 levels), and CSL-2D (49, 43, and 37 levels).

The harmonic distortion is calculated using the weighted total harmonic distortion (WTHD) of the voltages generated by the converter, given by

$$WTHD(\%) = \frac{100}{\gamma_1} \sqrt{\sum_{h=2}^{N_h} \left(\frac{\gamma_h}{h}\right)^2} \qquad (5)$$

where γ_1 is the fundamental voltage amplitude, γ_h is the corresponding harmonic component amplitude of the hth order, and N_h is the number of considered harmonics ($N_h = 1000$).

As N_{lvl} is the maximum number of voltage levels generated when $m_a = 1$, it is worthwhile to mention that the number of voltage levels actually generated decreases when m_a decreases. Fig. 6 shows the WTHD of the topologies with several values of m_a. CSL-1D has the best WTHD results, while CHB has the worst WTHD values. This outcome was expected, as the harmonic distortion decreases with the increase in the number of voltage levels. CSL-2D has an intermediate WTHD

result. When CSL-2D has two dc power sources, these WTHD values are always valid. When CSL-2D has only one dc power source, the floating capacitor needs to be regulated.

When CSL-2D with $N_{leg} = 6$ has $N_{lvl} = 43$ and 37, the floating capacitor can be regulated using only voltage levels redundancies when $0.45 \leq m_a \leq 0.93$ and $m_a \leq 0.99$, respectively (see section VI). In this case, the regulation is done without increasing the WTHD. CSL-2D can also operate with the modulation indexes that make the dc link b mean power equals zero. In these points, dc link b is naturally regulated and the best voltage levels are utilized most of the time (keeping the WTHD values good).

C. Power Losses and Switching Frequencies

The semiconductor losses analysis of the investigated configurations was obtained using PSIM's Thermal Module and the power device utilized in this analysis is SKM50GB063D from SEMIKRON. In addition, the transformers losses have been estimated using the methodology presented in [25]. Table VI shows the conduction, switching, transformers, and total losses ($P_{cd}, P_{sw}, P_{tr},$ and P_{to}, respectively) of the topologies. As the CSL-1D has the highest number of levels and consequently the lowest WTHD, its WTHD is taken as reference. A minimum sampling frequency (f_s) of 7.56 kHz is needed to synthesize its 63 levels, which produces a WTHD equals 0.0149%. The sampling frequency of the other topologies was adjusted so they also operate with a 0.0149% WTHD and these f_s values were utilized in the losses investigation.

Table VI compiles the power losses of the topologies, while Table VII shows the mean frequency of the switches of each leg over a complete period of the generated voltage in the same conditions as the losses investigation, as well as the sampling frequency applied. In these cases, it is considered that CSL-2D has two dc power sources and all topologies operate with $m_a = 1$.

TABLE VI
POWER LOSSES OF THE TOPOLOGIES WITH $v_{lWTHD} = 0.0149\%$, NORMALIZED IN RELATION TO P_l (OPERATION WITH $m_a = 1$ AND WITHOUT FLOATING CAPACITOR)

	CSL-2D ($N_{lvl} = 49/43/37$)	CSL-1D	CHB
P_{cd} (%)	1.153/1.152/1.153	0.502	0.449
P_{sw} (%)	0.195/0.155/0.181	0.815	1.120
P_{tr} (%)	4.000/3.990/3.990	4.090	4.250
P_{to} (%)	5.348/5.297/5.324	5.407	5.819

As converters a and b are connected in series, CSL-2D has the highest conduction losses. CSL-2D has the lowest switching losses in part because converters a and b have lower dc-link voltages than CHB and CSL-1D. The switching frequency of converter a is considerably lower than the one of converter b. This also explains the good results of the topology in terms of switching losses. The largest portion of the switching losses is from converter b.

CSL-2D with $N_{lvl} = 43$ has the best results in terms of semiconductor losses and switching frequency. This happens
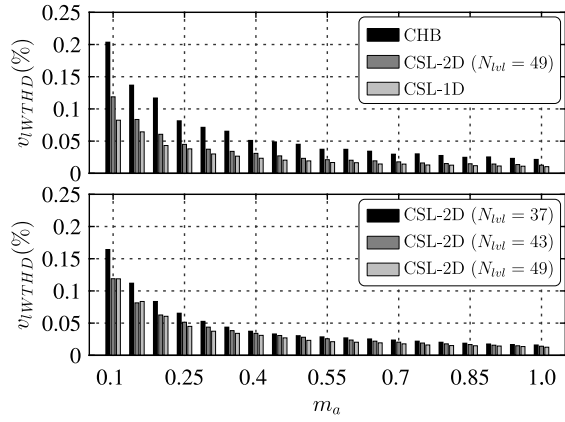
Fig. 6. v_{lWTHD} versus m_a when $f_s = 10.02\,\text{kHz}$ (N_{lvl} is the maximum number of voltage levels generated when $m_a = 1$).

TABLE VII
SAMPLING AND MEAN SWITCHING FREQUENCIES VALUES (KHZ) WITH $v_{lWTHD} = 0.0149\%$ (OPERATION WITH $m_a = 1$ AND WITHOUT FLOATING CAPACITOR)

Topology		Leg					Converter			f_s
	$s_a/s/$ $1,1$	$1_a/1/$ $2,1$	$2_a/2/$ $1,2$	$s_b/3/$ $2,2$	$1_b/4/$ $1,3$	$2_b/5/$ $2,3$	a	b	all	
CSL-2D										
49	0.06	0.45	1.26	1.62	4.85	11.32	0.59	5.93	3.26	9.00
N_{lvl} 43	0.06	0.18	0.42	0.78	4.49	11.65	0.22	5.64	2.93	9.54
37	0.06	0.18	0.42	0.78	4.49	12.31	0.22	5.86	3.04	10.74
CSL-1D	0.06	0.35	0.98	2.29	5.04	9.60	–	–	3.05	7.56
CHB	0.06	0.88	1.81	2.92	8.10	10.93	–	–	4.12	14.28

naturally regulating the floating capacitor. m_a values are 0.919, 0.9, and 0.912 when $N_{lvl} = 49$, 43 and 37, respectively, and the losses and switching frequencies results are shown in Tables VIII and IX. The maximum m_a with mean power in dc link b equals zero of CSL-2D with $N_{lvl} = 43$ and 37 can be increased to 0.934 and 0.937, respectively, at the cost of using redundancies that increase the mean frequency of the switches. As one can see, these results are still better than the ones of the CHB with $m_a = 1$.

TABLE VIII
POWER LOSSES OF CSL-2D WITH $v_{lWTHD} = 0.0149\%$, NORMALIZED IN RELATION TO P_l (OPERATION WITH THE MEAN POWER IN DC LINK b EQUALS ZERO)

	N_{lvl}		
	49	43	37
P_{cd} (%)	1.158	1.159	1.159
P_{sw} (%)	0.222	0.173	0.223
P_{tr} (%)	4.040	4.050	4.020
P_{to} (%)	5.420	5.382	5.402

TABLE IX
SAMPLING AND MEAN SWITCHING FREQUENCIES VALUES OF CSL-2D (KHZ) WITH $v_{lWTHD} = 0.0149\%$ (OPERATION WITH THE MEAN POWER IN DC LINK b EQUALS ZERO)

CSL-2D		Leg					Converter			f_s
N_{lvl}	s_a	1_a	2_a	s_b	1_b	2_b	a	b	all	
49	0.06	0.47	1.41	1.77	4.55	11.55	0.65	5.96	3.30	9.24
43	0.06	0.18	0.42	0.78	4.27	11.86	0.22	5.64	2.93	10.44
37	0.06	0.18	0.42	0.78	5.76	13.43	0.22	6.66	3.44	11.94

because it has more voltage levels redundancies that are utilized to decrease the mean switching frequency of each leg. Given that losses are very dependent on the operation point, the most suitable configuration depends on the application. Both CSL-2D and CSL-1D have better results than CHB. As CSL-1D has good results in terms of conduction losses, this topology is interesting for applications with high current. On the other hand, as CSL-2D has the lowest switching losses, this converter is a good option for application with high voltage. It is worth to mention that, CSL-2D has the lowest number of transformers and the lowest transformer losses.

The power losses and mean switching frequencies values were also analyzed considering that CSL-2D has a floating capacitor. In this case, CSL-2D operates with the maximum m_a that make the mean power in dc link b equals zero,

D. A comment on reliability

Define $V_l = 1$ p.u. and $N_{leg} = 6$. Consider CSL-2D operating with $m_a = 0.875$ and the dc-link voltage ratio $v_{Ca}/v_{Cb} = 7$ (i.e., $N_{lvl} = 49$). In this case, the dc-link voltages of CSL-2D are calculated as $v_{C_a} = (7/8)/0.875$ p.u. $= 1$ p.u. and $v_{C_b} = (1/8)/0.875$ p.u. $= 0.143$ p.u. On the other hand, consider CHB and CSL-1D with $m_a = 1$. Their dc-link voltages are calculated as $v_C = 1$ p.u. As $v_{Ca} = 1$ p.u., CSL-2D can be rearranged to work only with the converter a during a faulty condition in converter b. Consequently, the reliability of CSL-2D can be improved by the operation with a lower modulation index (in this case, $m_a = 0.875$). The same idea can be applied to CSL-2D with $N_{lvl} = 43$ and $N_{lvl} = 37$.
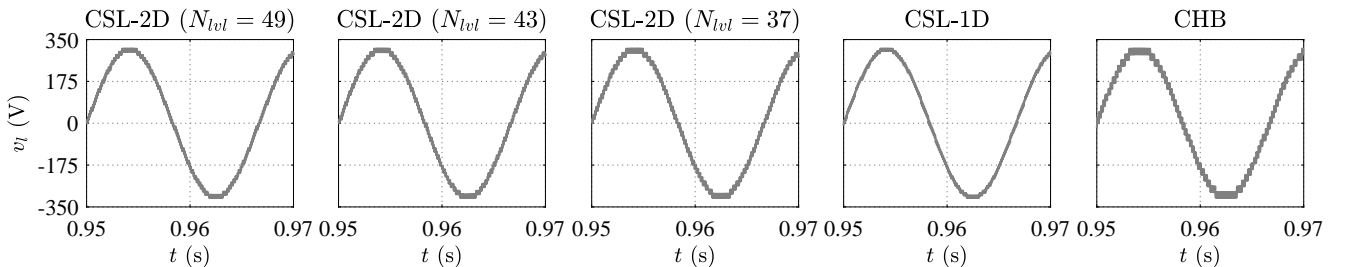

Fig. 5. Voltages synthesized by CSL-2D (49, 43, and 37 levels), CSL-1D (63 levels), and CHB (27 levels) using the parameters in Table III.
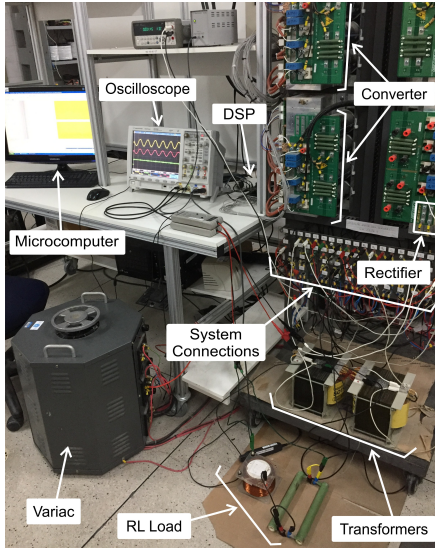
Fig. 7. Experimental setup.

Simulations were done to compare CSL-2D operating with lower modulation index and the conventional topologies operating with $m_a = 1$. The system parameters are the ones in Table III and CSL-2D operates without floating capacitor. Considering all topologies with the same mean WTHD as CSL-1D, CSL-2D with $m_a = 0.875$ and $N_{lvl} = 49$ has total semiconductor losses equals 1.404% of P_l. When CSL-2D operates with $m_a = 0.857$ and $N_{lvl} = 43$ ($v_{Ca}/v_{Cb} = 6$), the semiconductor losses are 1.340% of P_l. When $m_a = 0.833$ and $N_{lvl} = 37$ ($v_{Ca}/v_{Cb} = 5$), the semiconductor losses are 1.394% of P_l. Observing the results of CHB and CSL-1D from Table VI, CSL-2D has lower semiconductor losses than CHB and higher semiconductor losses than CSL-1D (it is worth noting that CSL-1D has more transformers than CSL-2D). Consequently, if it is desired to improve the reliability of CSL-2D, the topology could be designed to operate with lower modulation index. In this case, the converter b could be lost and the correct load voltage would still be generated.

VIII. SIMULATION AND EXPERIMENTAL RESULTS

Computer simulations and experimental results have been carried in the same operation conditions. The results were done with CSL-2D operating with $N_{leg} = 6$, $\eta_1 = 2/3$, $\eta_2 = 1/3$, and $v_{C_a} = 7v_{C_b}$. These values were obtained from the equations of Section III to maximize the number of generated voltage levels. Consequently, $N_{lvl} = 49$. The parameters utilized in the tests are provided in Table X. The experiments utilized a downscaled prototype that validates the PWM technique and the control strategy developed in this paper.

TABLE X
PARAMETERS USED IN SIMULATIONS AND EXPERIMENTAL TESTS OF CSL-2D

Parameter		Value
Reference load voltage	V_l^*	110 V(rms)
Dc-link voltages	v_{C_a}, v_{C_b}	148.75, 21.25 V
Transformers turns ratios	η_1, η_2	2/3, 1/3
Load modulation index	m_a	0.919
Dc-link capacitances	C_a/C_b	2200 μF
Load frequency	f_l	60 Hz
Sampling frequency	f_s	10 kHz

In order to verify and support the simulation and theoretical analysis, the CSL-2D converter has been built and investigated in laboratory. The experimental setup used during the tests is shown in Fig. 7. The main components of the workbench are highlighted in the image. A variac and a single-phase rectifier with a diode bridge provide the dc power supply. The power stage of the converter includes devices from SEMIKRON, with the switches being IGBT legs with dedicated drivers (SKHI23). Each converter (a or b) has a dc-link capacitance bank of 2200 μF rated at 900 V. The legs, sensors, dc source, and dc-link connections are located below the converter's modules. The RL load and transformers are at the bottom of the figure. A digital signal processor (DSP) TMS320F28335 with plug-in boards and sensors are used to gating signals generation and to measure variables.

The CSL-2D topology was evaluated with $m_a = 0.919$ and four different load conditions:

- case 1: RL load (load resistance and inductance $R_l = 27~\Omega$ and $L_l = 7$ mH, respectively) with $\cos \varphi = 0.99$;
- case 2: RL load ($R_l = 10~\Omega$ and $L_l = 60$ mH, respectively) with $\cos \varphi = 0.404$;
- case 3: non-linear load;
- case 4: load variation (an RL load had a 37.6% current step increase).

The startup results of CSL-2D with $m_a = 0.919$ and the load of case 1 are shown in Figs. 8a (simulation) and 9a (experiment). Note that during the simulations the floating capacitor reaches the correct value in less than two cycles of the generated voltage, while during the experiments it takes about two cycles. A larger view of the voltage synthesized in the same conditions is shown in Figs. 8b (simulation) and 9b (experiment). As one can see, the load voltage is multilevel, as expected.
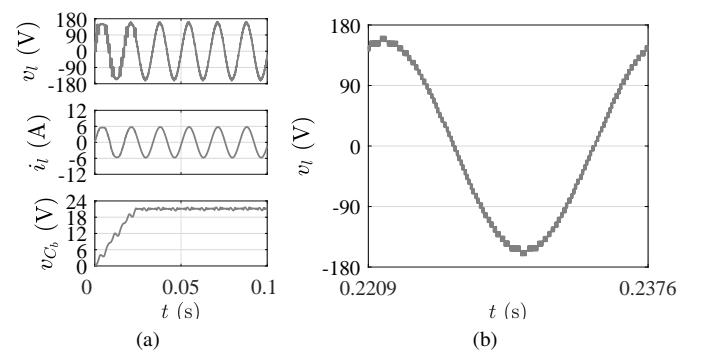

Fig. 8. Simulation of CSL-2D with $N_{leg} = 6$, $N_{lvl} = 49$, $m_a = 0.919$, and load of case 1. (a) Start-up. (b) Larger view of v_l.

The simulations and experimental results in each load condition are shown in Figs. 10 and 11, respectively. In cases 1, 2, and 3, the steady-state operation of the system is evaluated. As one can see, the voltage of the floating capacitor (v_{C_b}) is well regulated, even when the load is non-linear or has a
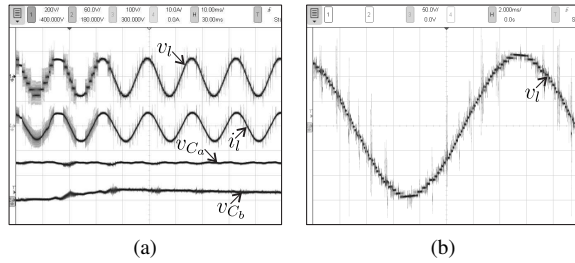
Fig. 9. Experimental results of CSL-2D with $N_{leg} = 6$ and $N_{lvl} = 49$, $m_a = 0.919$, and load of case 1. (a) Start-up (v_{C_a} with 100 volts/division, v_{C_b} with 60 volts/division, v_l with 200 volts/division, and i_l with 10 amperes/division). (b) Larger view of v_l (v_l with 50 volts/division).

low power factor. In case 4, the dynamical performance of the system during a step increase in the load is evaluated. Notice that all control requirements have been established.

The operation of CSL-2D with low modulation indexes and the same load as in case 1 is also shown in Figs. 12 (simulation) and 13 (experiment). The m_a utilized are some values in which the mean power in dc link b is approximately zero and this guarantees the operation with the best voltage levels most of the time. Notice that all control requirements have been established again.
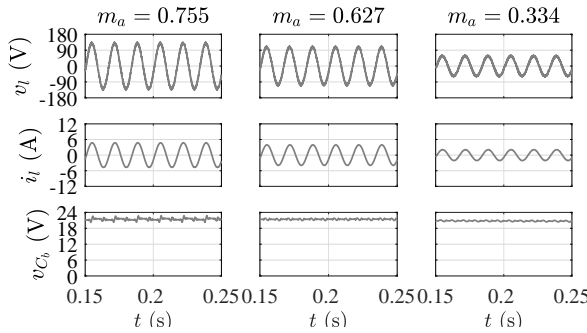
Fig. 12. Simulation of CSL-2D with $N_{leg} = 6$, $N_{lvl} = 49$, and load of case 1 with low modulation index.
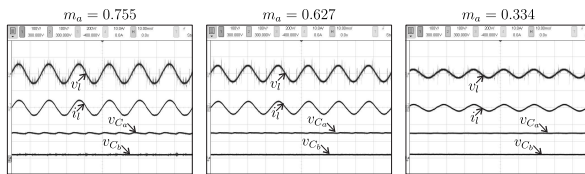
Fig. 13. Experimental results of CSL-2D with $N_{leg} = 6$, $N_{lvl} = 49$, and load of case 1 with low modulation index (v_{C_a} and v_{C_b} with 100 volts/division, v_l with 200 volts/division, and i_l with 10 amperes/division).

IX. Conclusions

In this paper, we have proposed a multilevel single-phase converter and its generalization. The basic configuration has six two-level IGBT legs (two legs are shared), two injection transformers and two dc links. Its lowest voltage dc link may be a floating capacitor or a small dc power source. The converter was applied as an inverter and compared with the conventional cascaded H-bridge and a generalized single-phase shared leg converter with one dc link. Compared with the conventional configurations, the proposed one has more levels

per transformer/leg when the configurations have the same number of legs/transformers. The converters were compared in terms of several parameters. Simulations were performed to compare the converters in terms of harmonic distortions of the generated voltages and power losses. The proposed topology has better power losses results when operating with high voltages and low currents. Experimental results were provided to demonstrate the feasibility of the system.

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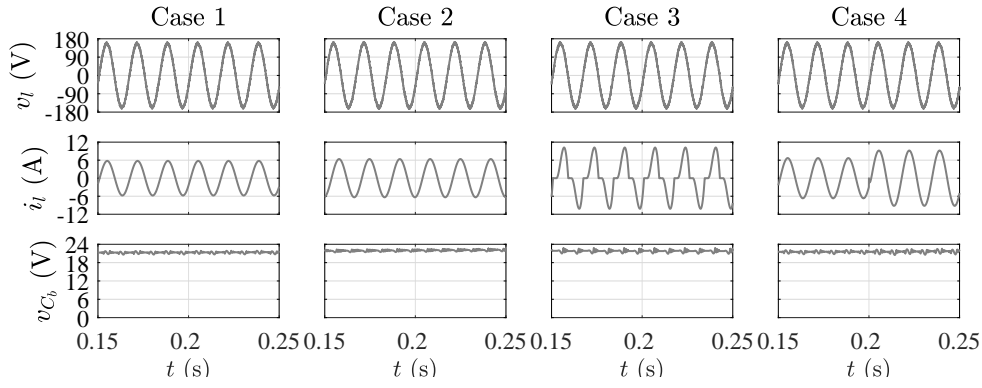
Fig. 10. Simulation of CSL-2D with $N_{leg} = 6$, $N_{lvl} = 49$, and $m_a = 0.919$. Case 1: RL load with $\cos \varphi = 0.99$; Case 2: RL load with $\cos \varphi = 0.404$; Case 3: non-linear load; Case 4: load variation.
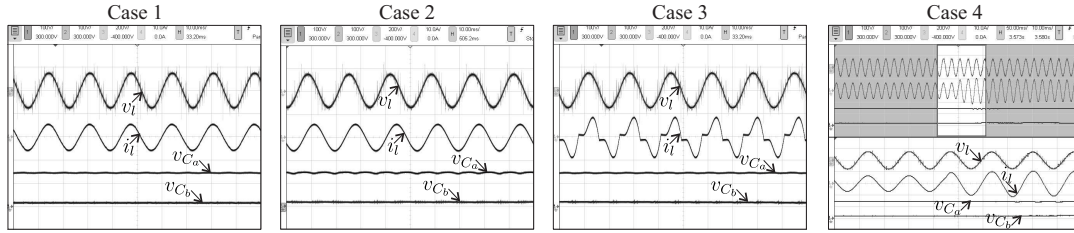

Fig. 11. Experimental results of CSL-2D with $N_{leg} = 6$, $N_{lvl} = 49$, and $m_a = 0.919$ (v_{C_a} and v_{C_b} with 100 volts/division, v_l with 200 volts/division, and i_l with 10 amperes/division). Case 1: RL load with $\cos \varphi = 0.99$; Case 2: RL load with $\cos \varphi = 0.404$; Case 3: non-linear load; Case 4: load variation.

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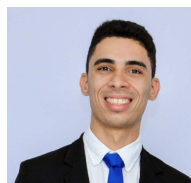
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